Hall Ticket Number:

Code No. : 13244 S

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (C.S.E/AIML) III-Semester Supplementary Examinations, July-2022

Logic and Switching Theory

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Define Boolean algebra? List out postulates and theorems of Boolean algebra?	2	1	1	1
2.	Reduce the following Boolean expression to the THREE literals: A'C' + ABC + AC'.	2	2	1	1,2
3.	"NAND and NOR gates are also called ad Universal gates", Justify it.	2	2	2	1,2
4.	Show that the dual of the exclusive-OR is also its complement.	2	2	2	1,2
5.	Compare encoders, priority encoders and multiplexers.	2	1	3	1
6.	Construct a 16x1 multiplexer with two 8x1 and one 2x1 multiplexers. Use the block diagram.	2	2	3	1,2
7.	Compare combinational circuit and sequential circuits.	2	1	4	1
8.	Construct a JK flip-flop using a D flip-flop, a 2-to-1-line multiplexer, and an inverter.	2	2	4	1,2
9.	List out the architectural differences between PROM, PLA, and PAL?	2	1	5	1
10.	Draw a PLA circuit to implement the following Boolean functions F = A'B + AC' + A'BC'	2	2	5	1,2
	Part-B (5 × 8 = 40 Marks)				
11. a)	Prove DeMorgan's theorems using truth table.	3	1	1	1,2
b)	Simplify Boolean function F(A, B,C,D,E) = ∑(0, 2, 4, 6, 9, 13, 21, 23, 25, 29, 31) using K-map.	5	3	1	1,2
12. a)	Draw a NAND logic diagram that implements the complement of the following function: F(A, B, C, D) = ∑(0, 1, 2, 3, 4, 8, 9, 12)	4	3	2	1,2
b)	Simplify the following expression to sum of product (SOP) using Tabulation Method: F(A, B, C, D) = m(0, 4, 8, 10, 12, 13, 15) + d(1,2)	4	3	2	1,2
13. a)	Explain the working of carry look ahead adder circuit.	3	2	3	1
b)	Design combinational circuit with three inputs and one output. The output is 1, when the binary value of the input is less than 3. The output is 0 otherwise.	5	3	3	1,2

Contd... 2

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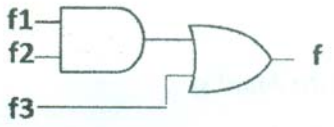
14. a)	Define Moore and Mealy finite state machine and explain with suitable example.	4	1	4	1
b)	Design a sequential circuit that accepts a serial bit stream 'X' as input and produces a serial bit stream 'Z' as output. Whenever the bit pattern "0110" appears in the input stream, it outputs Z=1; otherwise, Z=0.	4	3	4	1,2
15. a)	Tabulate the PLA programming table for the following Boolean functions listed below. Minimize the numbers of product terms. $F1(x, y, z) = \sum (1, 3, 5, 6)$ $F2(x, y, z) = \sum (0, 1, 6, 7)$	4	3	5	1,2
b)	Determine the PAL programming table for the BCD-to-Excess-3-Code converter, whose Boolean functions are simplified using following truth table:	4	3	5	1,2
16. a)	Convert following standard POS form to canonical POS form: $F1 = x'y + z' + xyz$ $F2 = A' + BC$	4	2	1	1,2
b)	Determine f2 in the following logic circuit, given that $f1 = \sum(4,5,6,7,8)$, $f3 = \sum(1,6,15)$ and $f = \sum(1, 6, 8, 15)$.	4	3	2	1,2
17.	Answer any ***two*** of the following:				
a)	Design combinational circuit, that convert, a four-bit gray code to four-bit binary number. Implement the circuit with XOR gates.	4	3	3	1,2
b)	Design a 3-bit binary counter using T-FF that has a repeated sequence of 6 states: 000-001-010-011-100-101-110. Give the state table, state diagram & logic diagram.	4	3	4	1,2
c)	Given a 64 X 8 ROM chip with an enable input. Show the external connections necessary to construct a 256 x 8 ROM with four chips and a decoder.	4	2	5	1,2

Input BCD				Output Excess-3 Code			
A	B	C	D	w	x	y	z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0



M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	19%
ii)	Blooms Taxonomy Level – 2	29%
iii)	Blooms Taxonomy Level – 3 & 4	52%

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